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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/667,601	09/23/2003	Dureseti Chidambarrao	FIS920030186US1	9755

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EXAMINER	
KENNEDY, JENNIFER M	

ART UNIT	PAPER NUMBER
2812	

DATE MAILED: 12/30/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/667,601	CHIDAMBARRAO ET AL.	
	Examiner	Art Unit	
	Jennifer M. Kennedy	2812	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *07 October 2004*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-16 and 21-23* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-16 and 21-23* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Response to Amendment

In view of Applicant's amendment to the claim, the objection of claim 11 is withdrawn.

In view of Applicant's amendment to the claim, the rejection of claim 9 under 35 U.S.C. 112 second paragraph, as being indefinite, is withdrawn.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claims 1 and 23 are rejected under 35 U.S.C. 102(e) as being anticipated by Sayama et al. (U.S. Patent Appl. 2004/0097030).

Sayama et al. disclose the method of forming an integrated circuit comprising a plurality of semiconductor devices including an n-type transistor and a p-type transistor on a semiconductor wafer, the method comprising:

covering the p-type transistor with a mask (see Figure 7); and

oxidizing a portion of a gate polysilicon of the n-type transistor, such that tensile mechanical stresses are formed within a channel of the n-type transistor (see [0036]-0038] and [0095-0097]).

The examiner considers the step of oxidizing to include formation of 90a and 40.

Further, Sayama et al. disclose wherein the step of oxidizing a portion of a gate polysilicon of the n-type transistor results in formation of a bird's beak in an edge of the gate polysilicon (see [0095]-[0097] and Figure 21)

The examiner notes that the rejection under Sayama et al. of claim 1 was only provided to properly reject newly added claim 23, which depends from claim 1.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1, 3-5, 12, 14-16 and 22 are rejected under 35 U.S.C. 103(a) as being unpatentable over Doyle et al. (U.S. Patent No. 6,288,694).

Doyle et al. teach in one embodiment the method of forming an integrated circuit comprising a plurality of semiconductor devices including an n-type transistor and a p-type transistor on a semiconductor wafer, the method comprising:

covering the p-type transistor with a mask and creating voids such that tensile mechanical stresses are formed within a channel of the n-type transistor without

creating additional tensile stresses in a channel of the p-type transistor (see Figures 5-7, column 4, lines 40-55, Figure 11, column 5, lines 5-25, and claims 1 and 5).

Doyle et al. does not teach in that embodiment that the voids are formed by oxidizing a portion of a gate polysilicon of the n-type transistor. Doyle et al. disclose in an additional embodiment that voids are formed by oxidizing a portion of the gate polysilicon of the n-type transistor (see column 5, line 40 through column 6, line 3). It would have been obvious to one of ordinary skill in the art at the time the invention was made to form the voids by oxidizing a portion of the gate polysilicon since Doyle et al. teach it is an alternative method of forming the voids that creates a tensile stress which increases the carrier mobility of the NMOS device.

In re claim 3 and 5, Doyle et al. disclose the method wherein the step of oxidation is performed by using low temperature oxidation, about 25 degrees C to about 600 degrees C, as defined by applicant (see column 5, lines 60-65). The examiner notes that the annealing step may be considered a part of the oxidation step since it allows for formation of the voids. Further, if the annealing process is not considered part of the oxidation step, then examiner notes that the oxidation step is performed at a temperature below that of the annealing temperature (400 degrees C), and thus is also considered a low temperature oxidation process.

In re claim 4, Doyle et al. disclose the method wherein the step of oxidation is performed by at least one of high pressure oxidation or atomic oxidation or plasma oxidation. The examiner notes that since oxygen atoms are being implanted it is considered an atomic oxidation step.

In re claim 12, Doyle et al. disclose the method of removing the mask used to cover the p-type field effect transistor (see column 5, lines 66-67).

In re claims 14 and 15, Doyle et al. does not disclose the range of tensile stress created in the n-type FET. The examiner notes that Applicant does not teach that the tensile stress range solve any stated problem or are for any particular purpose. Therefore, the tensile stress range lacks criticality in the claimed invention and does not produce unexpected or novel results. Thus, it would have been obvious to one of ordinary skill in the art at the time the invention was made to form the NFET with a tensile stress range as claimed, since the invention would perform equally well as long as sufficient tensile stress is applied to the NMOS region to increase the carrier mobility, as Doyle et al. teach, and because it has been held that where the general conditions of a claim are disclosed in the prior art, discovering the optimum or workable ranges involves only routine skill in the art. *In re Aller,* 105 USPQ 233, MPEP 2144.05 II A.

In re claim 22, Doyle et al. teach the method wherein the tensile stresses are formed along a longitudinal direction of the channel of the n-type transistor. The examiner notes that the longitudinal direction is arbitrary. The examiner maintains that stresses are created in the channel, and thus are formed along a longitudinal direction of the channel of the n-type transistor.

Claims 2 is rejected under 35 U.S.C. 103(a) as being unpatentable over Doyle et al. (U.S. Patent No. 6,288,694) in view of Khan et al. (U.S. Patent No. 4,517,731).

Doyle et al. disclose the method as claimed and rejected above including forming a mask of photoresist, but does not disclose the method wherein the mask is made of nitride.

Khan et al. disclose the method wheirn a mask is made of nitride. It would have been obvious to one of ordinary skill in the art at the time the invention was made to form the mask of Doyle et al. with nitride since as Khan et al. teach silicon nitride is less expensive, more reliable and much easier to work with as compared with the use of photoresist.

Claims 1, 3-16 and 21-22 are rejected under 35 U.S.C. 103(a) as being unpatentable over Bai et al. (U.S. Patent No. 6,204,103) in view of Doyle et al. (U.S. Patent No. 6,288,694).

In re claims 1 and 16, Bai et al. disclose the method for forming an integrated circuit comprising a plurality of semiconductor devices including an n-type transistor and a p-type transistor on a semiconductor wafer. Bai et al. does not disclose the method of covering the p-type transistor with a mask and oxidizing a portion of a gate polysilicon of the n-type transistor, such that tensile mechanical stresses are formed within a channel of the n-type transistor without creating additional tensile stresses in a channel of the p-type transistor (see Figures 5-7, column 4, lines 40-55, Figure 11, column 5, lines 5-25, and claims 1 and 5).

Doyle et al. disclose the method of covering the p-type transistor with a mask and oxidizing a portion of a gate polysilicon of the n-type transistor, such that tensile

mechanical stresses are formed within a channel of the n-type transistor without creating additional tensile stresses in a channel of the p-type transistor (see Figures 5-7, column 4, lines 40-55, Figure 11, column 5, line 5, through column 6, line 3, and claims 1 and 5).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to cover the p-type transistor with a mask and oxidize the gate polysilicon of the n-type transistor, such that tensile mechanical stresses are formed within a channel of the n-type transistor without creating additional tensile stresses in a channel of the p-type transistor because as Doyle et al. teach increasing the tensile stresses in the NMOS region while preventing the increasing of the tensile stresses in the PMOS region increases carrier mobility (see column 3, lines 20-25, an d column 5, line 40 through column 6, line 5).

In re claim 3 and 5, Doyle et al. disclose the method wherein the step of oxidation is performed by using low temperature oxidation, about 25 degrees C to about 600 degrees C, as defined by Applicants (see column 5, lines 60-65). The examiner notes that the annealing step may be considered a part of the oxidation step since it allows for formation of the voids. Further, if the annealing process is not considered part of the oxidation step, then examiner notes that the oxidation step is performed at a temperature below that of the annealing temperature (400 degrees C), and thus is also considered a low temperature oxidation process.

In re claim 4, Doyle et al. disclose the method wherein the step of oxidation is performed by at least one of high pressure oxidation or atomic oxidation or plasma

oxidation. The examiner notes that since oxygen atoms are being implanted it is considered an atomic oxidation step.

In re claim 6, Bai et al. disclose the method of forming a planarized oxide layer on the semiconductor wafer (1516).

In re claim 7 and 8, Bai et al. disclose the method comprising removing silicide (1505) material from above the gate polysilicon of the n-type field effect transistor, and wherein the step of removing silicide material form above the gate polysilicon of the n-type field effect transistor comprises etching the silicide material form above the gate polysilicon of the n-type field effect transistor (see column 6, lines 50-62).

In re claim 9, Bai et al. disclose the method further comprising removing deposited oxide (1516) from above the gate polysilicon of the n-type field effect transistor by etching the deposited oxide from above the gate polysilicon of the n-type field effect transistor (see column 6, lines 50-55).

In re claim 10, Bai et al. disclose the method further comprising depositing silicide material on at least the portion of the gate polysilicon of the n-type field effect transistor (see column 6, line 63 through column 7, line 5).

In re claim 11, Bai et al. disclose the method wherein the step of depositing silicide forming material on at least the portion of the gate polysilicon of the n-type field effect transistor comprises depositing at least one of Co, Hf, Mo, Ni, Pd_2, Pt, Ta, Ti, W, and Zr (see column 6, line 63 through column 7, line 5).

In re claim 12, Doyle et al. disclose the method of removing the mask used to cover the p-type field effect transistor (see column 5, lines 66-67).

In re claim 13, Bai et al. disclose the method of depositing at least one of a silicide material or a nitride cap on at least the gate polysilicon of the n-type field effect transistor and removing silicide material or the nitride cap form above the gate polysilicon of the no-type field effect transistor prior to performing the step of oxidizing (see column 6, lines 50-63).

In re claims 14 and 15, Doyle et al. does not disclose the range of tensile stress created in the n-type FET. The examiner notes that Applicant does not teach that the tensile stress range solve any stated problem or are for any particular purpose. Therefore, the tensile stress range lacks criticality in the claimed invention and does not produce unexpected or novel results. Thus, it would have been obvious to one of ordinary skill in the art at the time the invention was made to form the NFET with a tensile stress range as claimed, since the invention would perform equally well as long as sufficient tensile stress is applied to the NMOS region to increase the carrier mobility, as Doyle et al. teach, and because it has been held that where the general conditions of a claim are disclosed in the prior art, discovering the optimum or workable ranges involves only routine skill in the art. *In re Aller,* 105 USPQ 233, MPEP 2144.05 II A.

In re claim 21, the combined Bai et al. and Doyle et al. disclose the method wherein the step of oxidizing a portion of a gate polysilicon of the n-type transistor is performed after silicidation of the gate polysilicon. The examiner notes that Bai et al. teach the silicidation n-type transistor is conventional. Doyle et al. teach that the oxidation can be made after the completion of a conventional NMOS (see column 5, lines 39-45).

In re claim 22, the combined Bai et al. and Doyle et al. disclose the method wherein the tensile stresses are formed along a longitudinal direction of the channel of the n-type transistor. The examiner notes that the longitudinal direction is arbitrary. The examiner maintains that Doyle et al. disclose the stresses are created in the channel, and thus are formed along a longitudinal direction of the channel of the n-type transistor.

Response to Arguments

Applicants' arguments filed October 7, 2004 have been fully considered but they are not persuasive.

Applicants argue that none of the many embodiments of Doyle et al. disclose the method of oxidizing a portion of the gate polysilicon such that tensile mechanical stresses are formed within the channel. The examiner disagrees. The examiner maintains that the disclosure of Doyle et al. is related to the method of forming tensile stresses within the NMOS transistors, including stresses created in any one of the regions of the source, drain, channel and gate, which causes stress and deformation of the substrate, including the channel region. This deformation affects the bandgap and increases the carrier mobility of the transistor. (see explanation column 3, lines 10 through column 43 and Figures 2A and 2B).

The examiner has relied upon the embodiment described in column 5, line 40 through column 6 line 3 to disclose the method of oxidizing a portion of the gate polysilicon to form tensile mechanical stresses within the channel. The examiner notes that although the embodiment relied upon discloses oxidizing the polysilicon gate, Doyle

et al. disclose that it is an alternative to implanting the substrate channel region in order to create tensile stress in an NMOS device and NMOS channel. Doyle et al. clearly state that the NMOS device is strained such that the NMOS achieves increased carrier mobility (created by tensile stress, see column 5, line 39 through column 6, line 3 and column 3, lines 20-26). Doyle et al. define an NMOS device as having a source, gate, drain and a channel region (see column 5, lines 39-45). Thus, it is clear that the whole NMOS device, including the channel is under tensile strain. The examiner also notes that applicant's own disclosure realizes that stress formed in a layer above the channel region creates stress within the channel region (see specification, page 5, last paragraph).

Applicants also argue examiner's rejection with the combination of Bai et al. and Doyle et al. Applicants have concluded that the examiner admits at pages 5 and 6 that neither Bai et al. nor Doyle et al. disclose the method of "covering the p-type transistor with a mask" and "oxidizing a portion of a gate polysilicon of the n-type transistor, such that tensile mechanical stresses are formed within a channel of the n-type transistor without creating additional tensile stresses in a channel of the p-type transistor". The examiner notes that the cited section of page 5 and 6 contained a typographical error and that it was clear that Doyle was relied upon to show these limitations as evident by the combination of the references and the citation of Figures, column, and line numbers of Doyle et al.

The examiner again notes that embodiment described in column 5, line 40 through column 6 line 3 of Doyle et al. to disclose the method of oxidizing a portion of

the gate polysilicon to form tensile mechanical stresses within the channel and points Applicants to the argument provided above.

Applicants also argue that the tensile stress applied to the n-type transistors would be caused by the voids themselves, and not by forces exerted by an oxidized polysilicon gate. The examiner notes that the voids are created by oxidizing the polysilicon gate (implantation of the gate with oxygen), and thus indeed, it is the oxidized polysilicon gate that creates the tensile stress.

Finally, applicants argue that the claimed range of is critical, citing passages within the specification. The examiner notes that nowhere in the specification is the range of 500Pa to 1000Pa or 700MPa cited as a critical range. The examiner notes that while many passages discuss the advantage of increased tensile stress, the passages do not state the criticality of the range. Further, on page 13, applicants state that "the **desired** stresses are tensile and add values **of the order of 200MPa** and above." First, the examiner notes again, that the claimed range is desired, not critical. Further, the examiner notes that applicant is teaching in this passage that 200MPa is sufficient and therefore the range of 500 to 1000Pa or 700MPa is not critical. Also, the examiner notes that the language of "of the order" suggests that the order of magnitude desired is within the hundreds. The examiner notes that Doyle et al. disclose a magnitude of hundred MPa (see column 3, lines 40-45).

Conclusion

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP

§ 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jennifer M. Kennedy whose telephone number is (571) 272-1672. The examiner can normally be reached on Mon.-Fri. 8:30-5:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, John Niebling can be reached on (571) 272-1679. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Jennifer M. Kennedy
Patent Examiner
Art Unit 2812

jmk